Figure 1
prior art

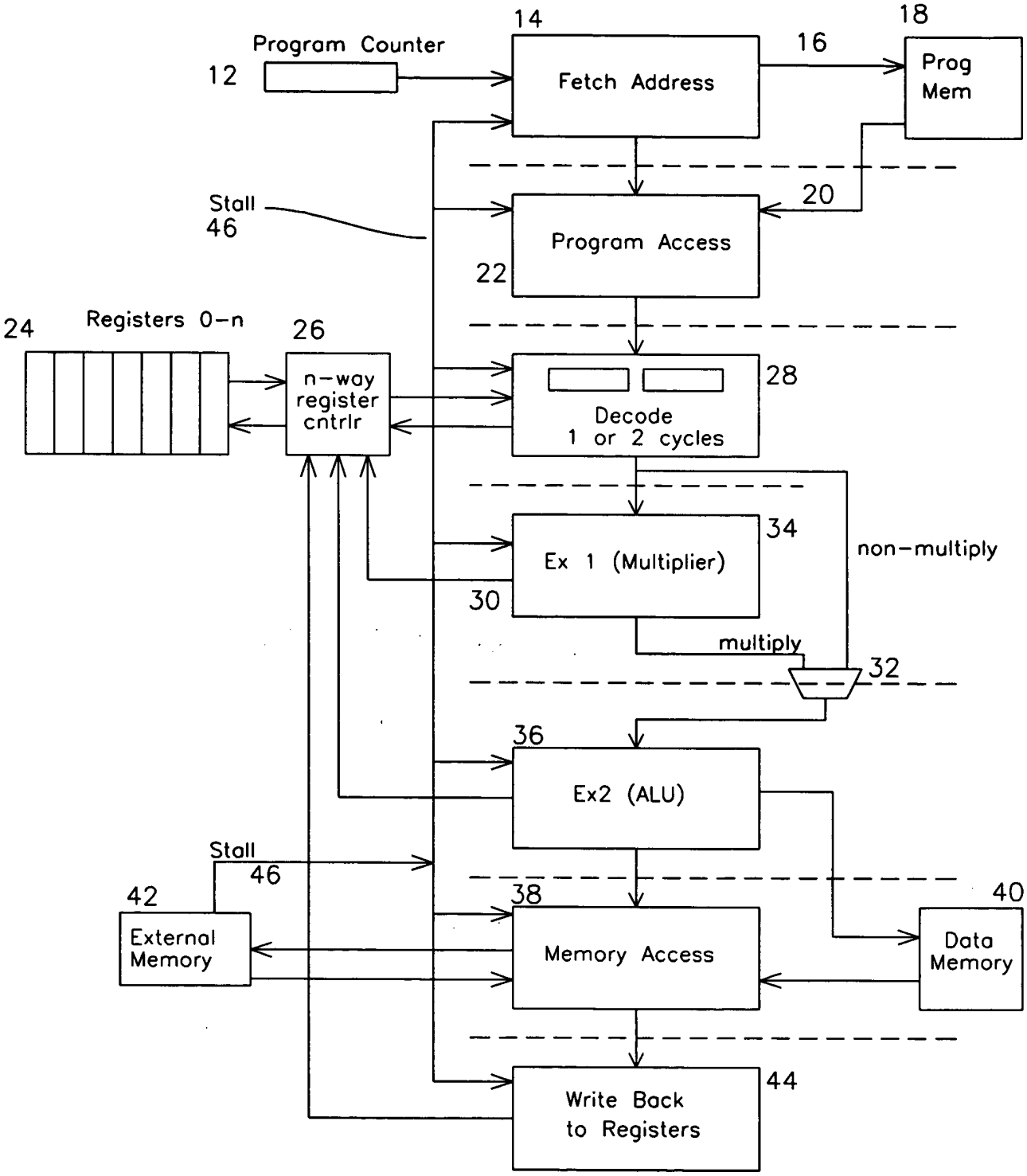

Figure 2

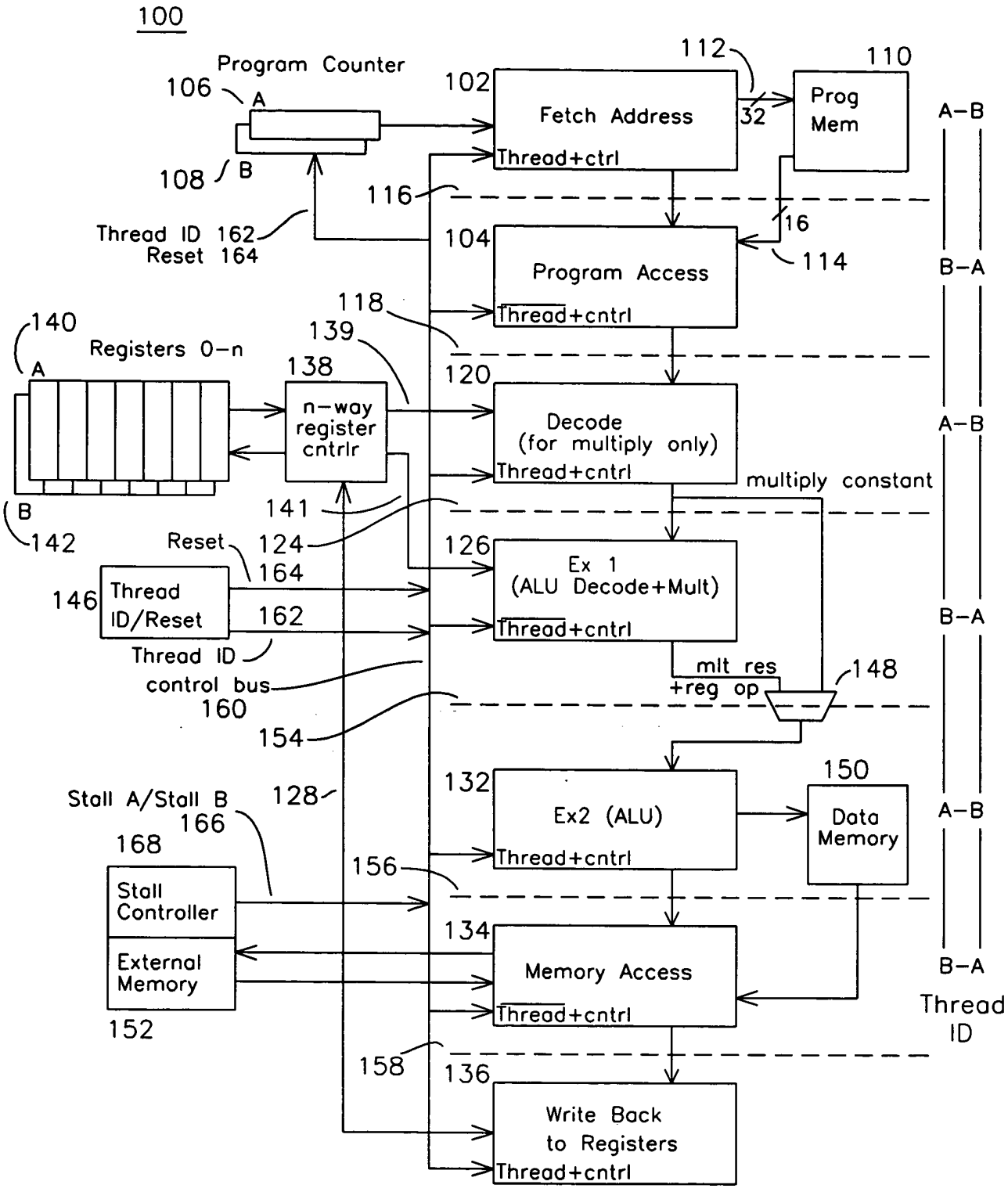
100
Program Counter
106
A
108
B
Thread ID 162
Reset 164
102
Fetch Address
Thread+ctrl
112
32
110
Prog Mem
A-B
116
16
104
Program Access
Thread+cntrl
114
B-A
118
140
Registers 0-n
A
139
138
n-way register cntrlr
120
Decode (for multiply only)
Thread+cntrl
A-B
multiply constant
B
142
141
124
Reset
164
126
Ex 1 (ALU Decode+Mult)
Thread+cntrl
146
Thread ID/Reset
162
Thread ID
control bus
160
B-A
mlt res +reg op
148
154
150
132
Ex2 (ALU)
Thread+cntrl
Data Memory
Stall A/Stall B
166
128
168
156
A-B
Stall Controller
External Memory
152
134
Memory Access
Thread+cntrl
B-A
Thread ID
158
136
Write Back to Registers
Thread+cntrl

Figure 3

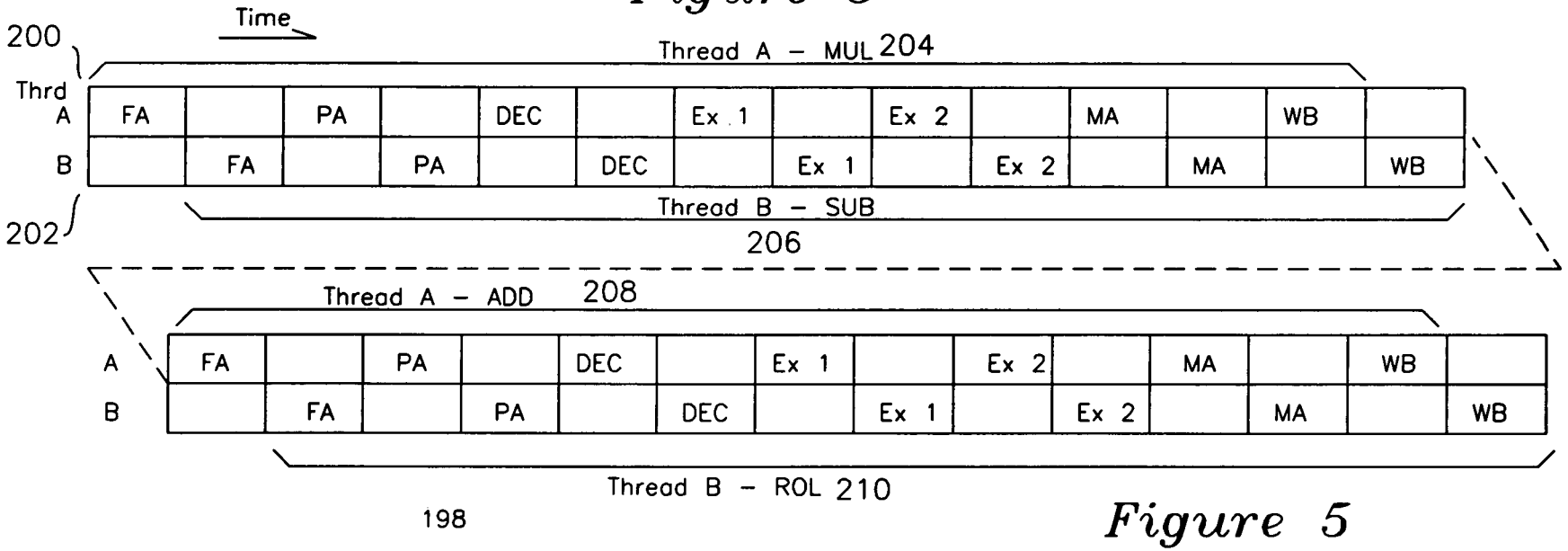

Figure 4

	216 Thread A	218 Thread B	
212	MUL D4, D5, D0	SUB D7, D6, D3	216
214	ADD D7,D3,D6	ROL D5, #3, D6	218
	MOV (D8)+,D13	ADDC D5, D4, D2	
	ROR D2, #1, D3	MAC D2, D3, D1	

Figure 5

220

222	FA	PA	DEC	EX1	EX2	MA	WB
Thread A	MUL						
Thread B	SUB	MUL					
Thread A	ADD	SUB	MUL				
Thread B	ROL	ADD	SUB	MUL			
Thread A	MOV	ROL	ADD	SUB	MUL		
Thread B		MOV	ROL	ADD	SUB	MUL	
Thread A			MOV	ROL	ADD	SUB	MUL
Thread B				MOV	ROL	ADD	SUB
Thread A					MOV	ROL	ADD
Thread B						MOV	ROL

Figure 6

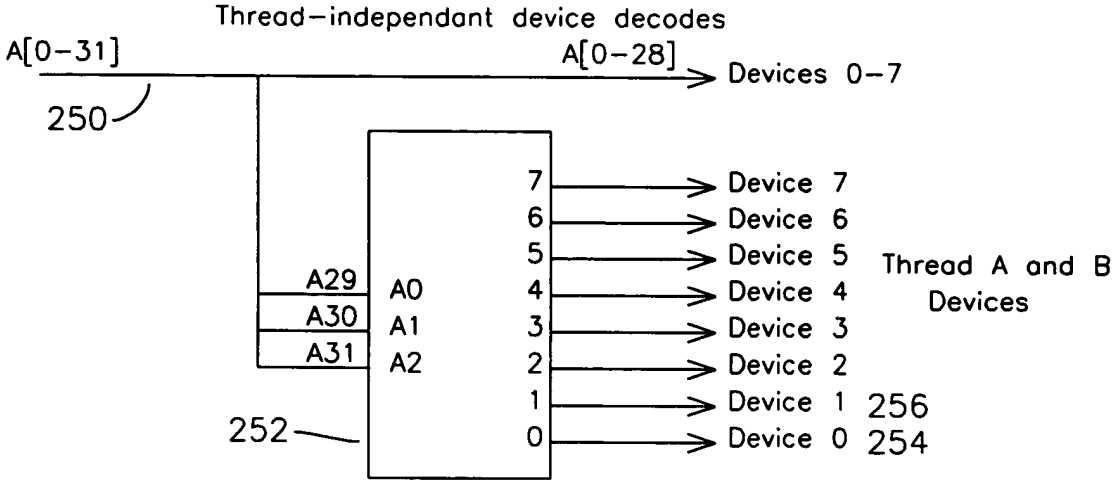

Figure 7